Time: 5 hours

Accomplishments:

* My board has arrived with a significant mistake in the CPLD layout. This was caused by neglecting to check the compatibility of the socket with the chip. Spent time meeting with Chandler to discuss options

Planned work:

* Find optimal solution for connecting CPLD to board.
* Solder remaining components to board.

Project % complete:

Hardware: 60%

Software : 2%